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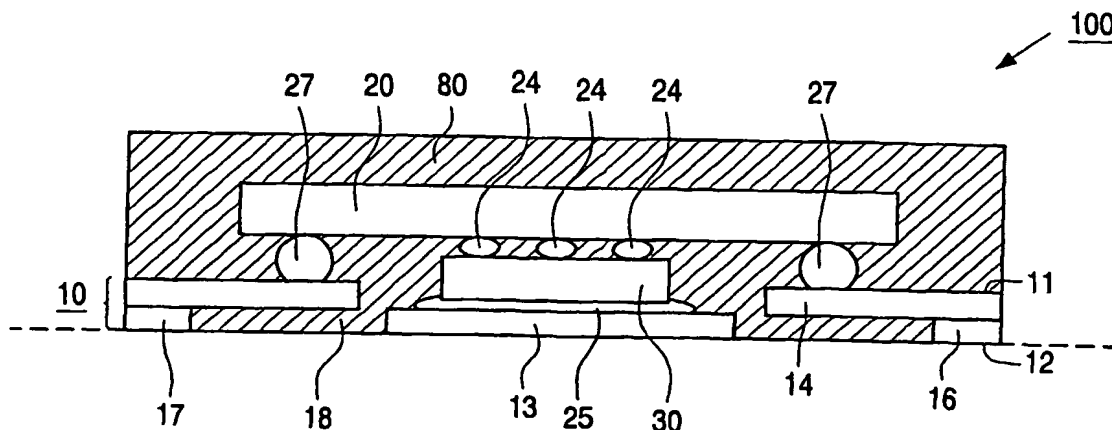
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[Continued on next page]

(54) Title: ELECTRONIC DEVICE AND METHOD OF MANUFACTURING SAME



(57) Abstract: The electronic device (100) is a chip-on-chip construction on a lead frame (10) comprising a heat sink (13) in an encapsulation (80). The first chip (20) and the second chip (30) are mutually connected by first conductive interconnections (24) and the first chip (20) is connected to the lead frame (10) by second conductive interconnections (27) which preferably have a lower reflow temperature than the first conductive interconnections (24). By heating the device (100) the adhesive layer (25) will first shrink, causing a stress, which will be relaxed by reflowing the second conductive interconnections (27).



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LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ,  
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**A. CLASSIFICATION OF SUBJECT MATTER**  
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**B. FIELDS SEARCHED**

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002/093087 A1 (PAEK JONG SIK) 18 July 2002 (2002-07-18) the whole document	1,8
A	US 2002/105789 A1 (CHAN LIEN-CHIH ET AL) 8 August 2002 (2002-08-08) the whole document	1,8
A	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 09, 30 September 1996 (1996-09-30) -& JP 08 125112 A (HITACHI LTD; HITACHI VLSI ENG CORP), 17 May 1996 (1996-05-17) the whole document	1,8
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☒ Patent family members are listed in annex.

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Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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